**Cell design flow**

* SC - standard cell placed in library
* Macros , IP’s , cells with different sizes is present in the library
* The sizes are referred to as drive strength threshold voltage decides the speed

There are three major steps

**Inputs**

* PDKs, DRC, LVS, SPICE models , user - defined specs
* Spice model parameter - given by foundry
* Cell height - separation between ground and power grill
* Cell width - decided by drive strength
* Supply voltage
* Metal layer
* Pin location
* Drawn gate length

**Design steps**

* Circuit design
* Implement the circuit
* Output - CDL file [circuit description language]

**Layout design**

* **Implement values and functions**
* Outputs - GDS II , LEF , extracted spice netlist (.cir)

**Characterization**

* Output – timing, noise, power
* Read in the models
* Read extracted spice netlist
* Recognise behaviour of buffer
* Read the subcircuit of the inverter
* Attach necessary power sources
* Apply the stimulus
* Necessary output capacitance
* Stimulation commands

**Timing characterization**

|  |  |
| --- | --- |
| Sl no | Characters |
| 1 | slew\_low\_rise\_thr |
| 2 | slew\_high\_rise\_thr |
| 3 | slew\_low\_fall\_thr |
| 4 | slew\_high\_fall\_thr |
| 5 | in\_rise\_thr |
| 6 | in\_fall\_thr |
| 7 | out\_rise\_thr |
| 8 | out\_fall\_thr |

**Propagation delay**

Time (out\_\*\_thr) -- Time (in\_\*\_thr)

**Transition time**

Rise high low

Fall high low